WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a plurality of memory cells each comprising:

a data storage section storing data; and

a transfer gate section having a MOSFET of a first conductive type for writing said data to said data storage section and reading said data from said data storage section,

wherein a potential corresponding to the data stored in said data storage section is applied as a substrate bias of said MOSFET.

2. The semiconductor memory device according to claim 1, wherein said transfer gate section includes a plurality of MOSFET's of the first conductive type connected in parallel.

3. The semiconductor memory device according to claim 1, wherein said data storage section includes a second MOSFET of the first conductive type, and

the second MOSFET has a source connected to a power supply and a drain connected to a source of a first MOSFET of said transfer gate section, a potential of a gate being applied as a substrate bias of the second MOSFET and a substrate bias of said first MOSFET.

4. The semiconductor memory device according to claim 3, wherein said transfer gate section includes a plurality of MOSFET's of the first conductive type connected in parallel.

5. The semiconductor memory device according to claim 1, wherein said data storage section includes first and second CMOS inverters cross-connected to each other,

a source of a first MOSFET of said transfer gate section is connected to an output terminal of said first CMOS inverter and a potential of the source of said first MOSFET is applied as a substrate bias of said second CMOS inverter, and

an output of said second CMOS inverter is applied as a substrate bias of said first MOSFET and a substrate bias

of said first CMOS inverter.

6. The semiconductor memory device according to claim 5, wherein said transfer gate includes a third MOSFET of the first conductive type,

the third MOSFET has a source connected to an output terminal of said second CMOS inverter, and

an output of said first CMOS inverter is applied as the substrate bias.

7. The semiconductor memory device according to claim 1, wherein said data storage section comprises:

a first resistor having one end connected to a first power supply and the other end connected to a source of a first MOSFET of said transfer gate;

a second MOSFET of the first conductive type having a drain connected to the source of said first MOSFET and a source connected to a second power supply;

a second resistor having one end connected to said first power supply and the other end connected to a gate of said second MOSFET; and

a third MOSFET of the first conductive type having a drain connected to the gate of said second MOSFET, a source connected to said second power supply, and a gate connected to a drain of said second MOSFET,

and wherein a gate potential of said second MOSFET is applied as a substrate bias of said first MOSFET and a substrate bias of said second MOSFET, and a gate potential of said third MOSFET is also applied as a substrate bias of said third MOSFET.

8. The semiconductor memory device according to claim 7, wherein said transfer gate section has a fourth MOSFET of the first conductive type, and

the fourth MOSFET has a source connected to a gate of said second MOSFET and applied with the gate potential of said third MOSFET as a substrate bias of the fourth MOSFET.

9. A semiconductor memory device comprising a plurality of memory cells each comprising:

first to fourth wells formed on a semiconductor substrate and isolated from one another;

a first MOSFET of a first conductive type formed in said first well, having a diffused layer becoming a drain and connected to one of a pair of bit lines, and having a gate connected to a word line;

a second MOSFET of the first conductive type formed in said first well, having a diffused layer becoming a drain, the diffused layer being a common diffused layer becoming a source of said first MOSFET;

a third MOSFET of the first conductive type formed in said second well, having a diffused layer becoming a drain and connected to the other bit line of the pair of bit lines, and having a gate connected to said word line;

a fourth MOSFET of the first conductive type formed in said second well, having a diffused layer becoming a drain, the diffused layer being a common diffused layer becoming a source of said third MOSFET;

a fifth MOSFET of a second conductive type formed in said third well, and having a gate common to the fifth MOSFET and said second MOSFET;

a sixth MOSFET of the second conductive type formed in said fourth well, and having a gate common to the sixth MOSFET and said fourth MOSFET;

a first wiring connecting a diffused layer becoming a source of said second MOSFET to a diffused layer becoming the drain of said fifth MOSFET;

a second wiring connecting a diffused layer becoming a source of said fourth MOSFET to a diffused layer becoming a drain of said sixth MOSFET;

a first contact section formed in an isolation region isolating said first well from said third well, and connecting said first wiring to the gates of said fourth and sixth MOSFET's; and

a second contact section formed in an isolation region

isolating said second well from said fourth well, and connecting said second wiring to the gates of said second and fifth MOSFET, wherein said first well is connected to said third well through the gates of said second and fifth MOSFET's, and

said second well is connected to said fourth well through the gates of said fourth and sixth MOSFET's.

10. The semiconductor memory device according to claim 9, wherein said first contact section and said second contact section are arranged to be opposed to each other.

11. The semiconductor memory device according to claim 9, wherein the diffused layers becoming the sources of said first and third MOSFET's are L-shaped.